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MS-7177

Version:0A

CPU:

Intel Tejas & Prescott LGA775 Processor

System Chipset:

Intel Grantsdale: 915GV/915PP/915G/910GL

Intel ICH6

On Board Chipset:

BIOS -- FWH EEPROM

AC'97 Codec -- ALC655

LPC Super I/O -- W83627THF Ver:E

LAN --RTL8100C/RTL8110S

CLOCK --Cypress 28416

Main Memory:

DDRII * 4

Expansion Slots:

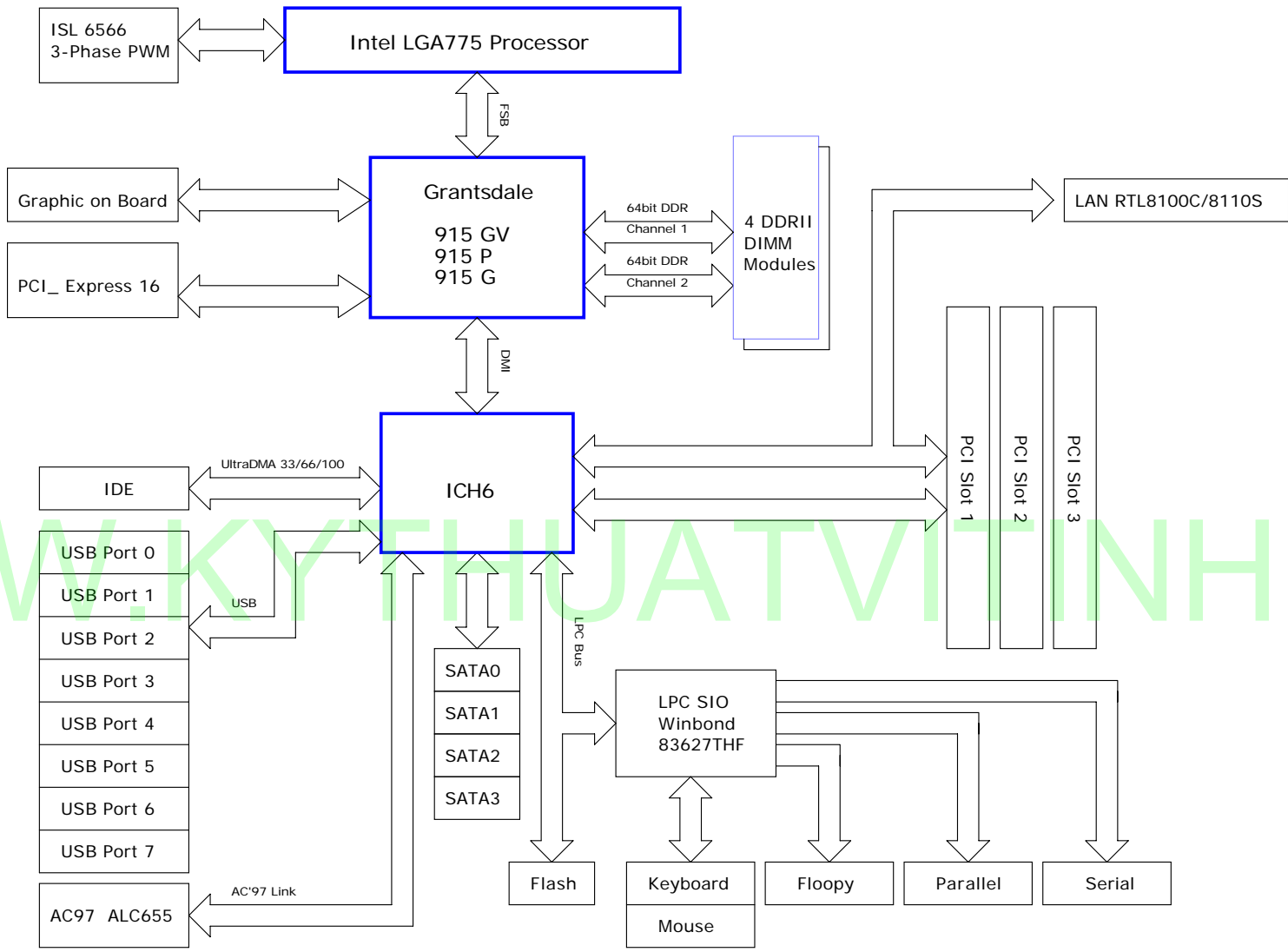
PCI EXPRESS X16 SLOT

PCI SLOT * 3

PWM:

Controller: Intersil 6566

Block Diagram



Tejas		
0.8375V - 1.6000V Core	-	95A
1.2V FSB Vtt	-	TBD A

Gransdale GMCH		
1.2V FSB Vtt	-	1.0A
1.8V DDRII I/O (S0,S1)	-	4.7A
1.8V DDRII I/O (S3)	-	25mA
*2.5V DAC	-	0.07A
2.5V HV	-	TBD A
1.5V Core (Integrated)	-	9.7A
1.5V Core (Discrete)	-	7.7A
*1.5V PCI Express	-	1.4A

ICH6		
1.2V VCC_CPU	-	tbdmA
1.5V Core	-	1.88A
*1.5V PCI Express	-	260mA
1.5V SATA	-	430mA
+3.3V VccSus	-	330mA
RTC (G3)	-	5uA
5VRef	-	TBD A
5VrefSus	-	TBD A
+3.3V	-	180mA

FWH		
+3.3V (S0,S1)	-	107mA

ISL6566		
VCCP	VRM 10.1	
0.8375V-1.6000V	95A	
3-Phase Switch		

W83310DS		
VTT_DDR		
1.3V Linear	1.0A	

MS7 Regulator		
V_FSB_VTT		
1.2V Linear	5.0A	
VCC_DDR		
1.8V (S0,S1)	8.0A	
Linear(S3)	570mA	
V_2P5_MCH		
2.5V Linear	100mA	
VCC3_SB		
3.3V Linear	1.5A	
5V DUAL1,2		
5V Linear	22mA	

MS6+ Regulator		
V_1P5_CORE		
1.5V Switch	14A	

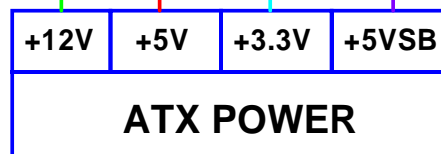
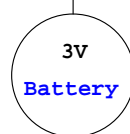
DDR DIMM & TERMINATOR		
0.9V VTT_DDR	-	1.2A
1.8V VCC_DDR (S0,S1)	-	9.4A
1.8V VCC_DDR (S3)	-	400mA

PCI Express x16 slot		
+12V	-	5.5A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

PCI slot x3		
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	7.6A
+5V	-	5.0A
+12V	-	0.5A

USB		
+5V (S0,S1)	-	4A
+5V (S3)	-	20mA

PS2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA



ICH6 Not modify yet

GPIO Pin	Type	Function	Power	Pin
GPIO 0	I	REQ#6 pull-up to VCC5 with 2.7K	5V	B7
GPIO 1	I	REQ#5 pull-up to VCC5 with 2.7K, and connect to RTL8100C	5V	E8
GPIO 2	I	PIRQ#E pull-up to VCC5 with 2.7K	5V	D9
GPIO 3	I	PIRQ#F pull-up to VCC5 with 2.7K	5V	C7
GPIO 4	I	PIRQ#G pull-up to VCC5 with 2.7K	5V	C6
GPIO 5	I	PIRQ#H pull-up to VCC5 with 2.7K	5V	M3
GPIO 6	I	GP16 pull-up to VCC3 with 10K	3.3V	AD19
GPIO 7	I	GP17 pull-up to VCC3 with 10K	3.3V	AE19
GPIO 8	I	GP18 pull-up to VCC3_SB with 10K	3.3V_SB	R1
GPIO 9	I	OC#3_4 connect to USB connector	3.3V_SB	C23
GPIO 10	I	OC#3_4 connect to USB connector	3.3V_SB	D23
GPIO 11	I	SMB_ALERT# pull-up to VCC3_SB with 10K	3.3V_SB	W6
GPIO 12	I	PS_DETECT pull-up to VCC3 with 10K	3.3V	M2
GPIO 13	I	SIO_PME# connect to LPC I/O	3.3V_SB	R6
GPIO 14	I	OC#3_4 connect to USB connector	3.3V_SB	C25
GPIO 15	I	OC#3_4 connect to USB connector	3.3V_SB	C24
GPIO 16	O	NC	3.3V	D8
GPIO 17	O	PGNT#5 connect to RTL8100C	3.3V	F6
GPIO 18	O	NC	3.3V	AC21
GPIO 19	O	BIOS_WP# connect to FWH	3.3V	AB21
GPIO 20	O	NC	3.3V	AD22
GPIO 21	O	NC	3.3V	AD20
GPIO 23	O	GPO23_TBL# connect to FWH	3.3V	AD21
GPIO 24	I/O	GPIO24 connect to Lenovo header	3.3V_SB	V3
GPIO 25	I/O	pull-down to GND with 1K directly (enable internal 2.5V VRM)	3.3V_SB	P5
GPIO 26	I	pull-up to VCC3 with 10K directly	3.3V	AF17
GPIO 27	I/O	GPIO27 connect to Lenovo header	3.3V_SB	R3
GPIO 28	I/O	NC	3.3V_SB	T3
GPIO 29	I	pull-up to VCC3 with 10K directly	3.3V	AE18
GPIO 30	I	pull-up to VCC3 with 10K directly	3.3V	AF18
GPIO 31	I	pull-up to VCC3 with 10K directly	3.3V	AG18
GPIO 32	I/O	LEO_CLKRUN#	3.3V	AF19
GPIO 33	I/O	NC	3.3V	AF20
GPIO 34	I/O	GPIO34 connect to Lenovo header	3.3V	AC18
GPIO 40	I	PREQ#4 pull-up to VCC5 with 2.7K	5V	F7
GPIO 41	I	NC	3.3V	P4
GPIO 48	O	NC	3.3V	E7
GPIO 49	OD	H_PWRGD pull-up to VTT_OUT_LEFT with 100 ohm, and connect to CPU	VCPU	AG25

FWH

GPIO Pin	Type	Function
GPIO 0	I	PD_DET

PCI Configuration

DEVICE	INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 2	INTB# INTC# INTD# INTA#	PCI_REQ#1 PCI_GNT#1	AD18	PCICLK1
PCI Slot 3	INTC# INTD# INTA# INTB#	PCI_REQ#2 PCI_GNT#2	AD19	PCICLK2
PCI Slot 1	INTD# INTA# INTB# INTC#	PCI_REQ#3 PCI_GNT#3	AD20	PCICLK3
LAN	INTH#	PCI_REQ#5 PCI_GNT#5	AD27	LAN_CLK

PCI RESET DEVICE

Signals	Target
PLTRST#	Grandstale, MS7
PCIRST_ICH6#	PCIE_16, LAN
PCIRST#1	FWH, SIO, LEO Header
PCIRST#2	PCI Slot 1, 2, 3
HD_RST#	IDE

DDR DIMM Config.

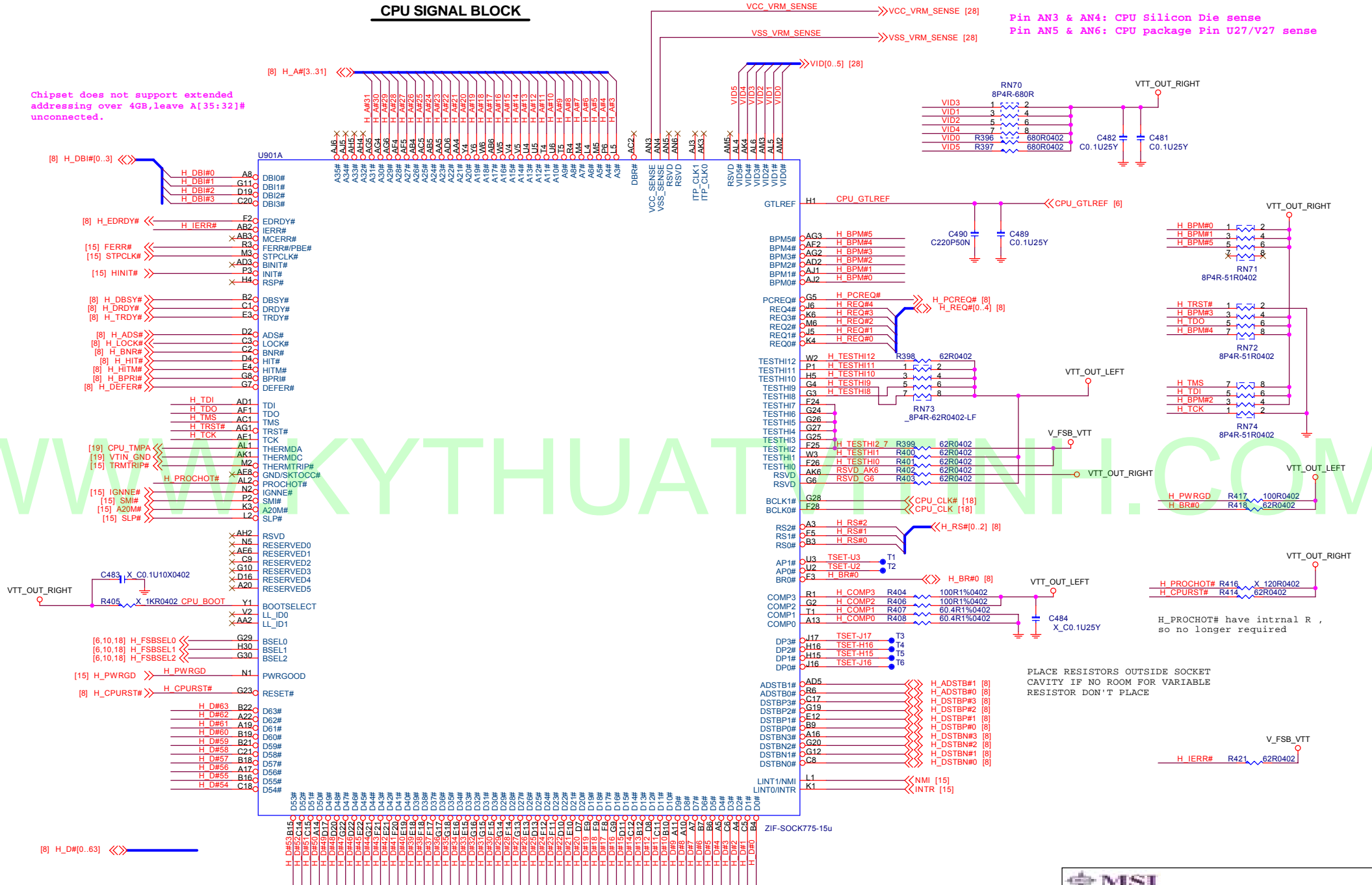
DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A4H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2

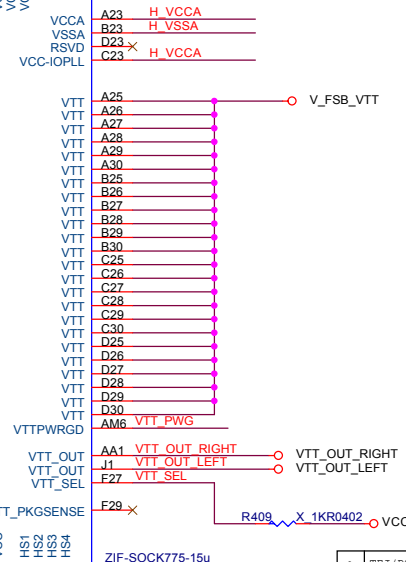
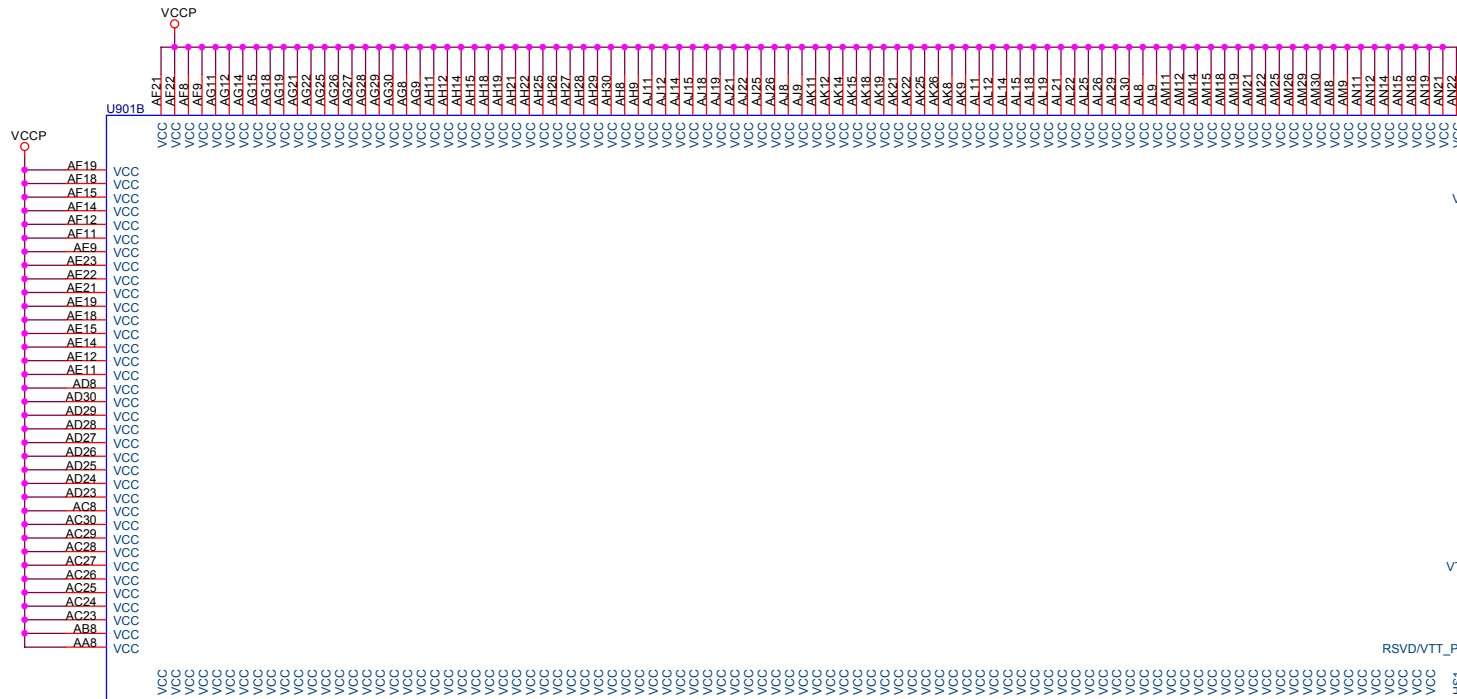
JUMPER SETTING

RTCST	(2-3) NORMAL	(1-2) CLEAR
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CPU SIGNAL BLOCK

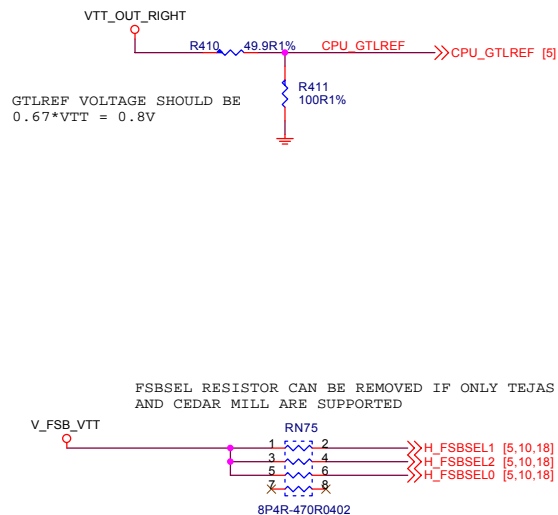
Chipset does not support extended addressing over 4GB, leave A[35:32]# unconnected.



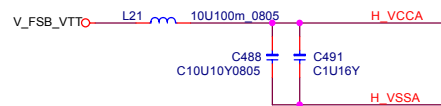


0	TEJ / PSC
1	RSVD

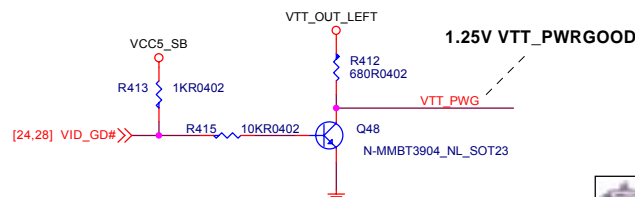
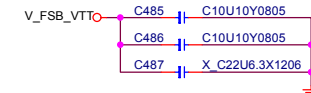
Pin F27: VTT_SEL Output Pin
VTT_SEL = 1 for the Pentium 4 processor
in the 775-land package.



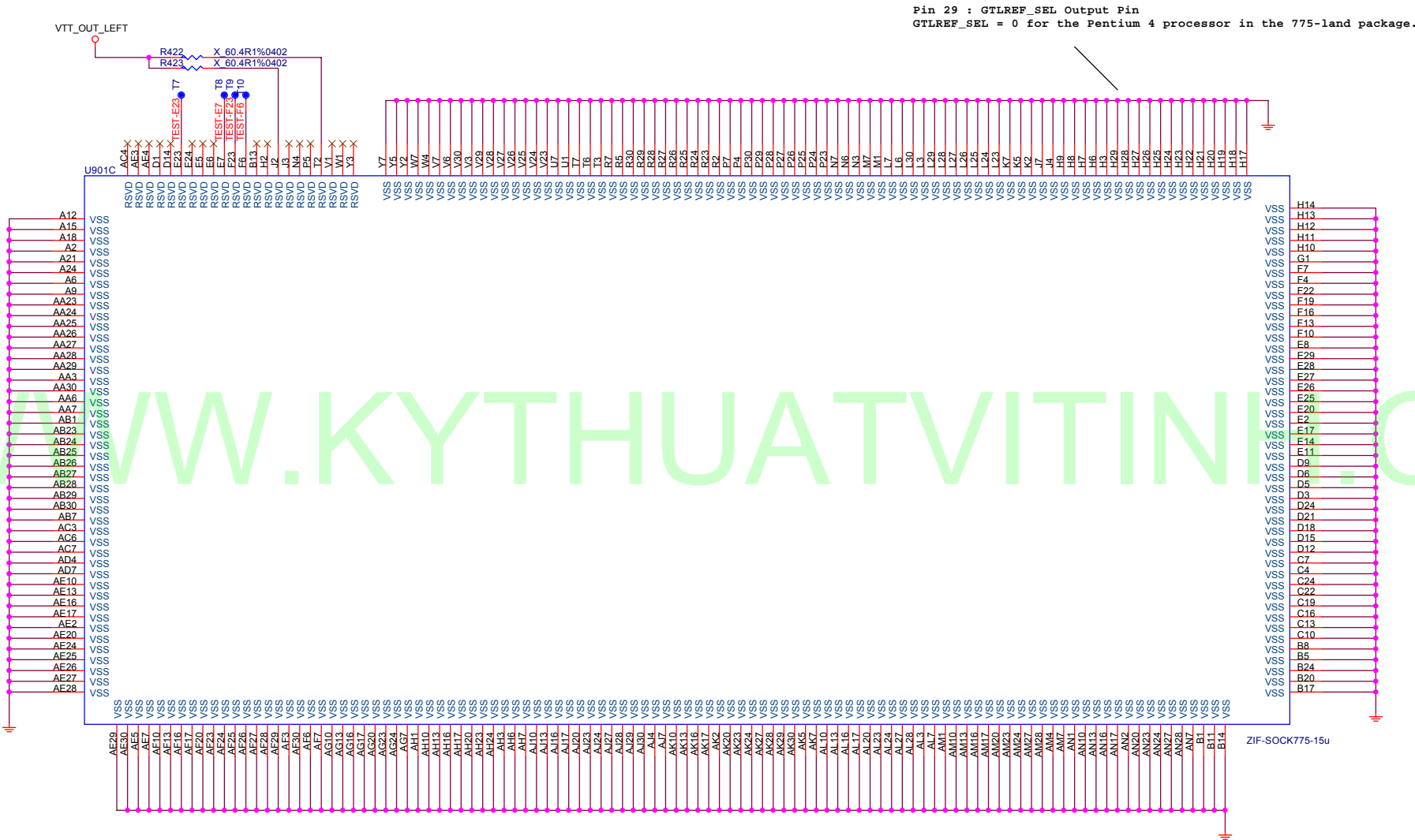
PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
TRACE WIDTH TO CAPS MUST BE SMALLER THAN 12MILS

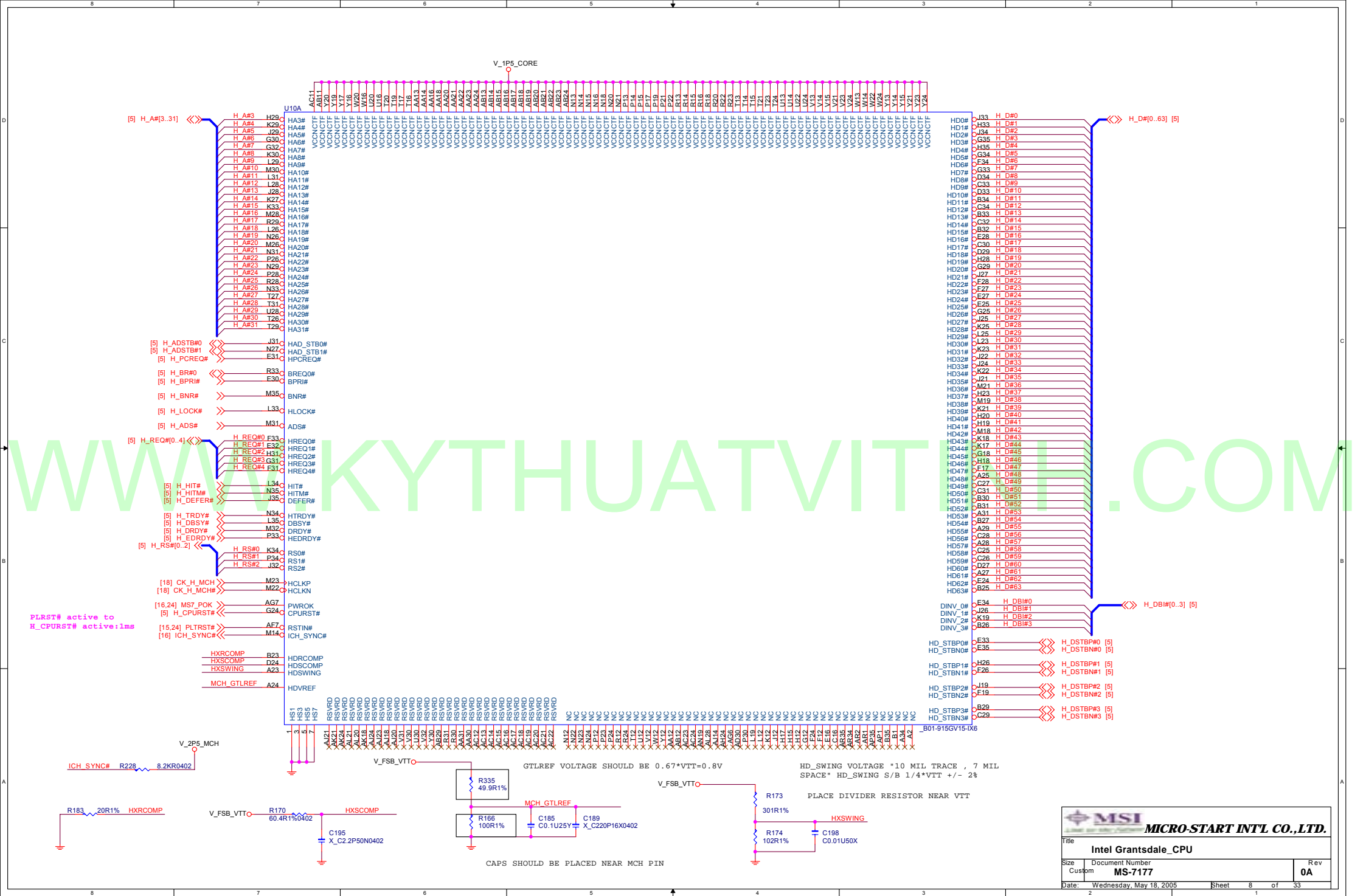


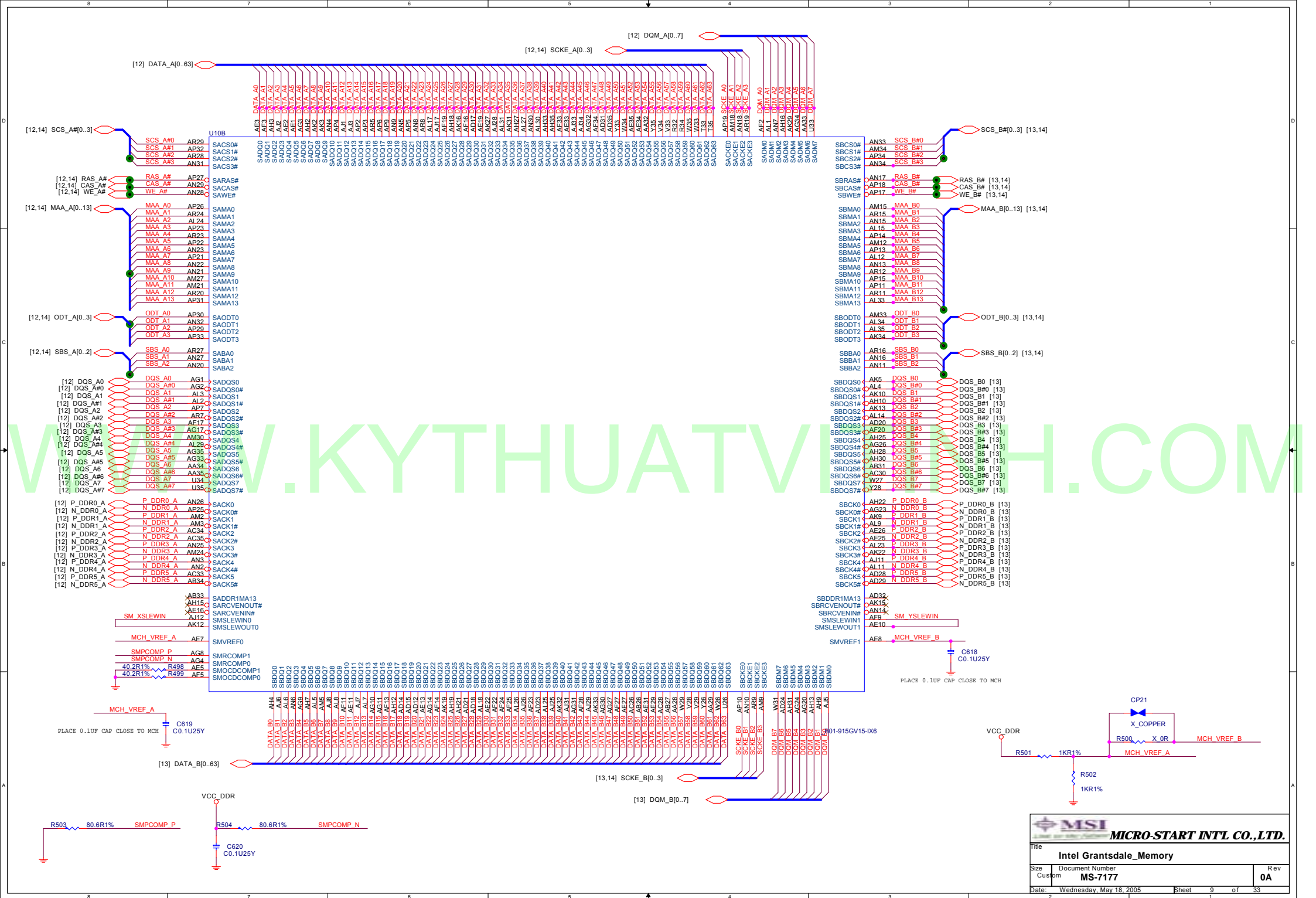
CAPS FOR FSB GENERIC

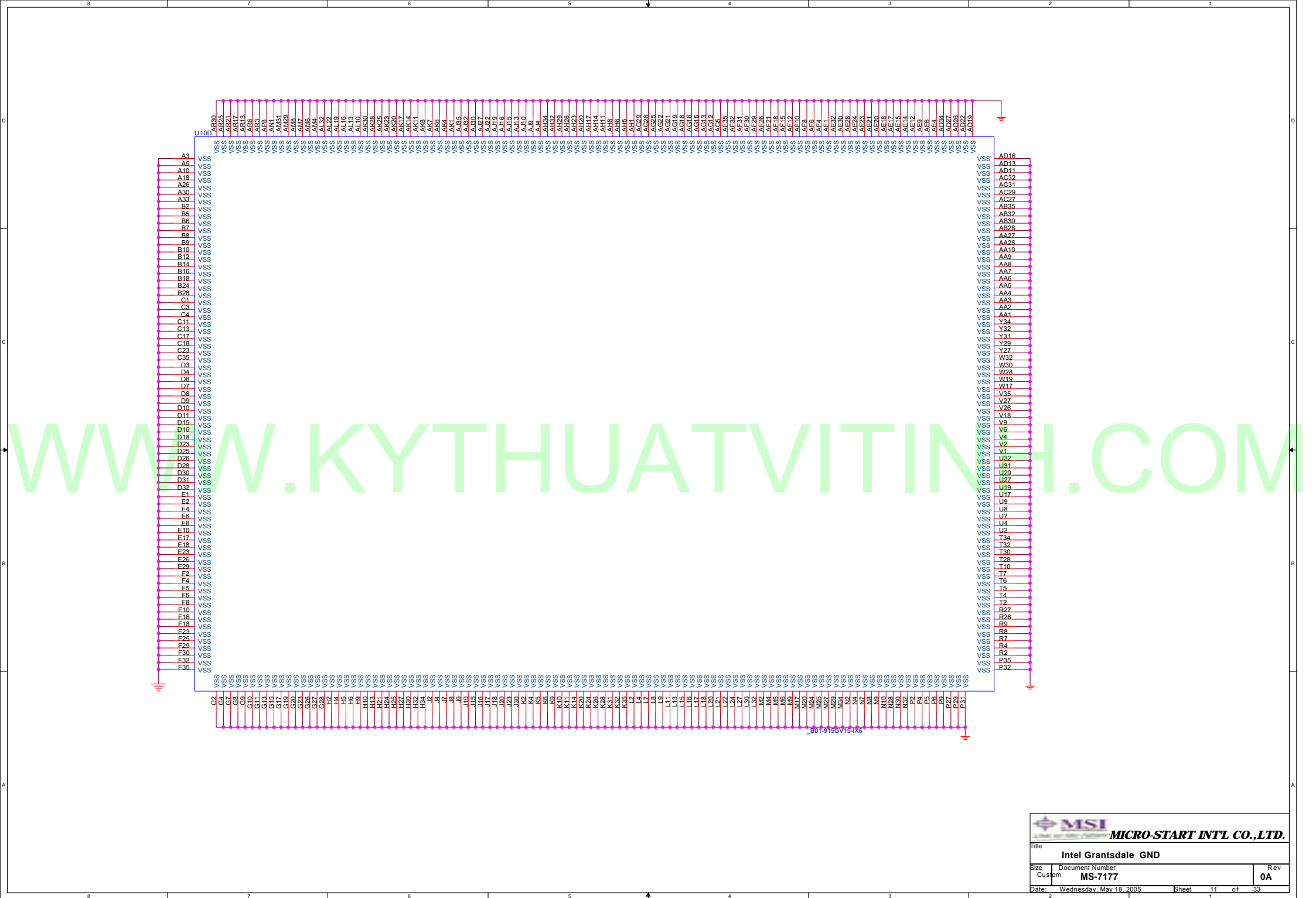


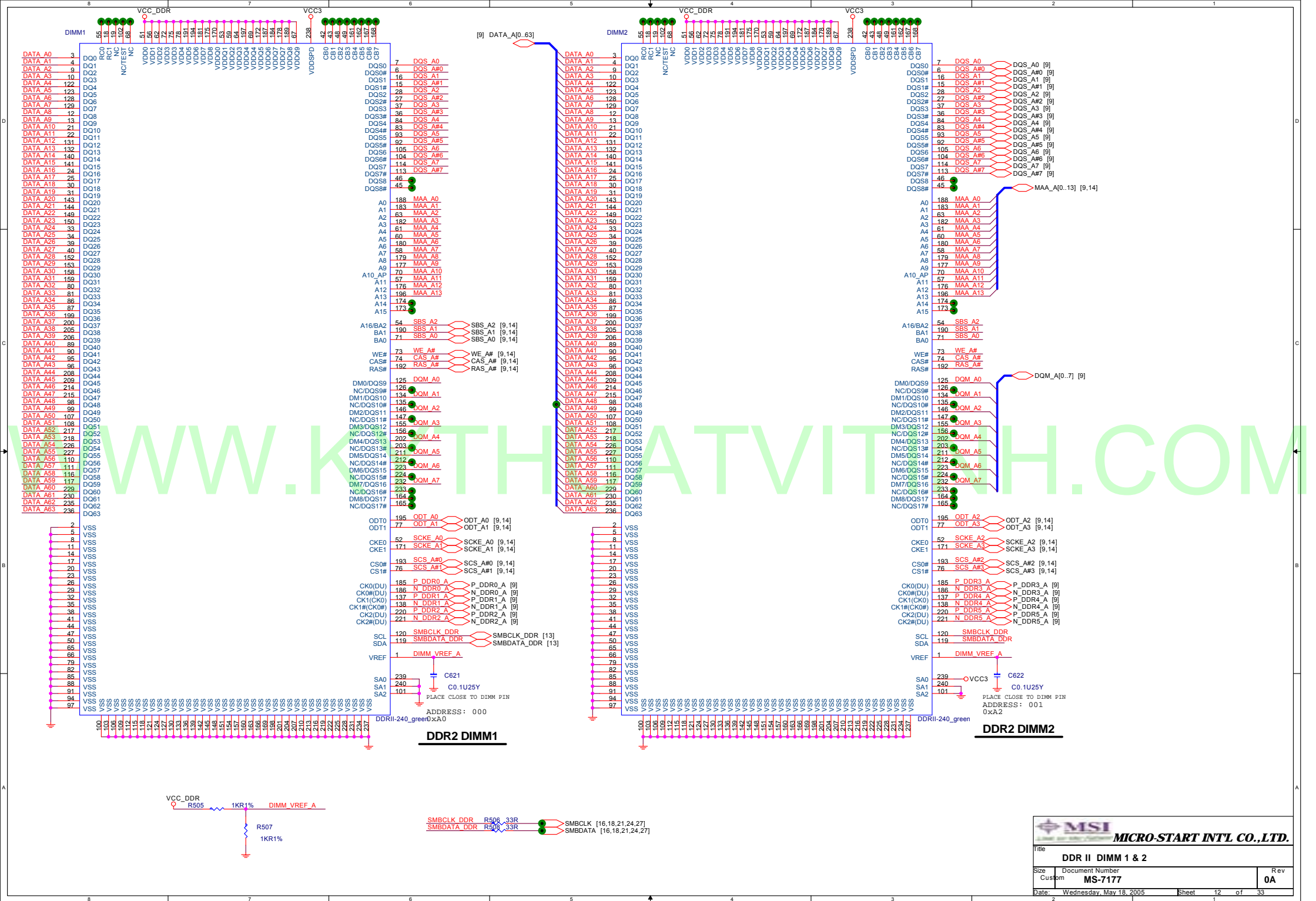
MICRO-START INT'L CO.,LTD.		
Title Intel LG775 - Power		
Size Custom	Document Number MS-7177	Rev 0A
Date: Wednesday, May 18, 2005	Sheet 6	of 33

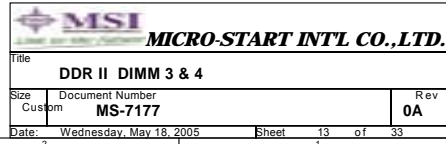


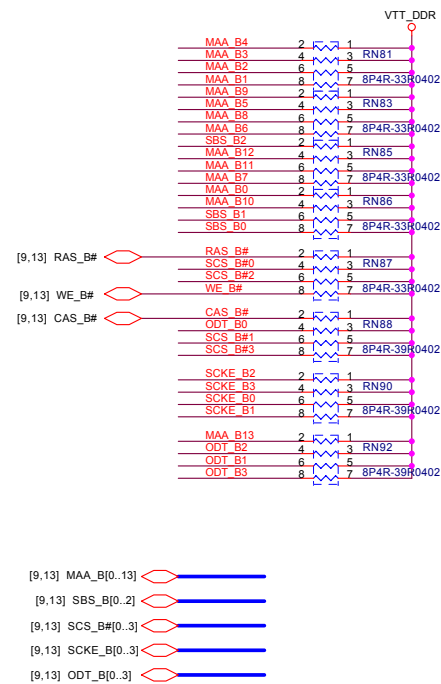
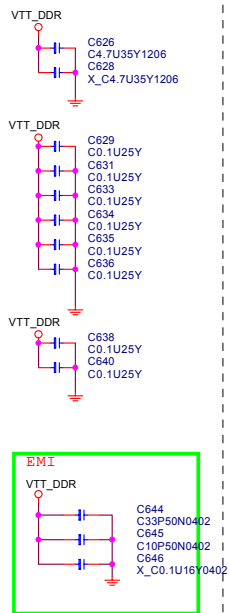




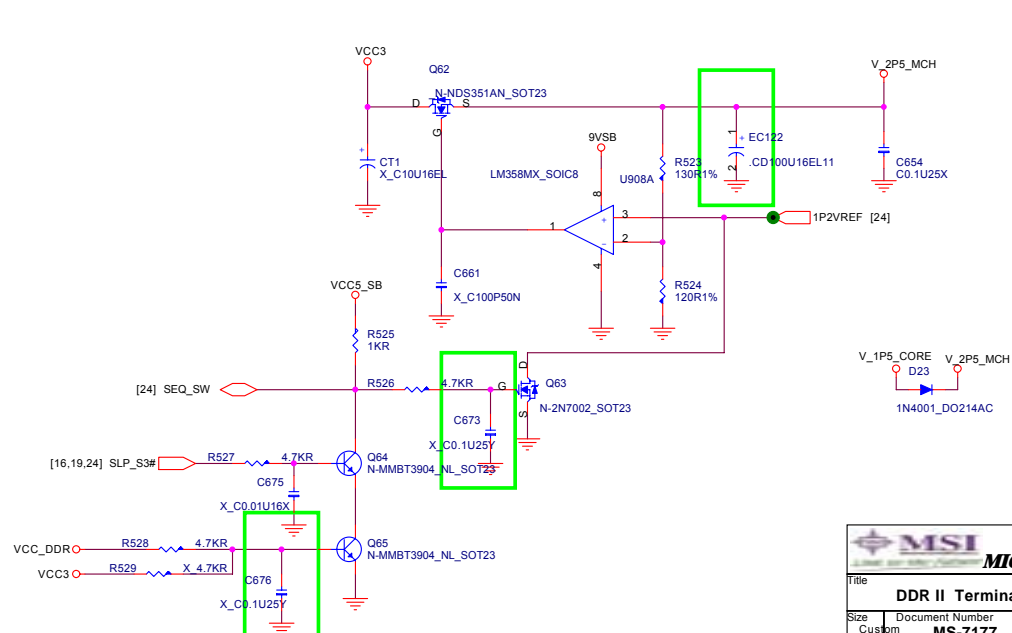
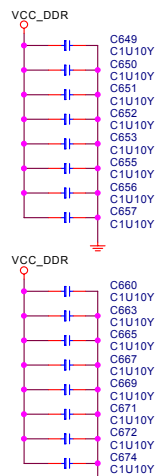








Grantsdale GMCH Power Sequencing Requirement
Between 1.5V Core and 2.5V DAC



U15A

[23.27] AD[31..0] <<

[23.27] C_BE#[3..0] <<

[23.27] DEVSEL# <<

[23.27] FRAME# <<

[23.27] IRODY# <<

[23.27] TRDY# <<

[23.27] STOP# <<

[23.27] PAR# <<

[23.27] LOCK# <<

[23.27] SERR# <<

[23.27] PERR# <<

[23.27] PME# <<

[18] ICH_PCLK <<

[21.27] PCIRST_ICH6# <<

[23] PREQ#0 <<

[23] PREQ#1 <<

[23] PREQ#2 <<

[23] PREQ#3 <<

[23] PREQ#4 <<

[23.27] PREQ#5 <<

[23.27] PREQ#6 <<

[23] PGNT#1 <<

[23] PGNT#2 <<

[23] PGNT#3 <<

[27] PGNT#5 <<

[23] PIQ#A <<

[23] PIQ#B <<

[23] PIQ#C <<

[23] PIQ#D <<

[23] PIQ#E <<

[23] PIQ#F <<

[23] PIQ#G <<

[23.27] PIQ#H <<

[19.29] SERIRQ <<

[22] IRQ14 <<

XX1 <<

XX2 <<

XX3 <<

XX4 <<

_B01-801FB65-1X6

PCI INTERFACE

ICH 6
PART 1/3

CPU

PCI EXPRESS

DIRECT MEDIA

LAN

INTERRUPT

A20M# << AE23 >> A20M# [5]
 CPUSLP# << AE27 >> SLP# [5]
 FERR# << AE24 >> FERR# [5]
 IGNNE# << AG26 >> IGNNE# [5]
 INIT# << AE27 >> HINIT# [5]
 INIT3_3V# << AE22 >> FWH_INIT# [18]
 INTR << AG24 >> INTR [5]
 NMI << AE26 >> NMI [5]
 SM# << AG27 >> SM# [5]
 STPCLK# << AE26 >> STPCLK# [5]
 RCIN# << AD23 >> KBRST# [19]
 A20GATE << AE22 >> A20GATE [19]
 THRMTRIP# << AE23 >> TRMTRIP# [5]
 GPO49/CPUPWRGD << AG25 >> H_PWRGD [5]

PLTRST# << R5 >> PLTRST# [8.24]

PERN_1 << H25 >>

PERP_1 << H24 >>

PETN_1 << G27 >>

PETP_1 << G26 >>

PERN_2 << K25 >>

PERP_2 << K24 >>

PETN_2 << J27 >>

PETP_2 << J26 >>

PERN_3 << M25 >>

PERP_3 << M24 >>

PETN_3 << L27 >>

PETP_3 << L26 >>

PERN_4 << P24 >>

PERP_4 << P23 >>

PETN_4 << N27 >>

PETP_4 << N26 >>

DMI_0RXN << T26 >>

DMI_0RXP << T24 >>

DMI_0TXN << R27 >>

DMI_0TXP << R26 >>

DMI_1RXN << V25 >>

DMI_1RXP << V24 >>

DMI_1TXN << U27 >>

DMI_1TXP << U26 >>

DMI_2RXN << V25 >>

DMI_2RXP << Y24 >>

DMI_2TXN << W27 >>

DMI_2TXP << W26 >>

DMI_3RXN << AB24 >>

DMI_3RXP << AB23 >>

DMI_3TXN << AA27 >>

DMI_3TXP << AA26 >>

DMI_CLKN << AD25 >>

DMI_CLKP << AC25 >>

DMI_ZCOMP << F24 >>

DMI_IRCOMP << F23 >>

LAN_CLK << F12 >>

LAN_RSTSYNC << B11 >>

LAN_RXD0 << E12 >>

LAN_RXD1 << E11 >>

LAN_RXD2 << C13 >>

LAN_TXD0 << C12 >>

LAN_TXD1 << C11 >>

LAN_TXD2 << E13 >>

EE_CS << D12 >>

EE_DIN << F13 >>

EE_DOUT << D11 >>

EE_SHCLK << B12 >>

VSS_1 << A1 >>

VSS_2 << A2 >>

VSS_3 << A3 >>

VSS_4 << A4 >>

VSS_5 << A5 >>

VSS_6 << A6 >>

VSS_7 << A7 >>

VSS_8 << A8 >>

VSS_9 << A9 >>

VSS_10 << A10 >>

VSS_11 << A11 >>

VSS_12 << A12 >>

VSS_13 << A13 >>

VSS_14 << A14 >>

VSS_15 << A15 >>

VSS_16 << A16 >>

VSS_17 << A17 >>

VSS_18 << A18 >>

VSS_19 << A19 >>

VSS_20 << A20 >>

VSS_21 << A21 >>

VSS_22 << A22 >>

VSS_23 << A23 >>

VSS_24 << A24 >>

VSS_25 << A25 >>

VSS_26 << A26 >>

VSS_27 << A27 >>

VSS_28 << A28 >>

VSS_29 << A29 >>

VSS_30 << A30 >>

VSS_31 << A31 >>

VSS_32 << A32 >>

VSS_33 << A33 >>

VSS_34 << A34 >>

VSS_35 << A35 >>

VSS_36 << A36 >>

VSS_37 << A37 >>

VSS_38 << A38 >>

VSS_39 << A39 >>

VSS_40 << A40 >>

ICH6 Pull-Up / Down Resistors

KBRST# RN55 8P4R-10KR0402
 A20GATE 1 2
 SERIRO 3 4
 THRM# 5 6
 THRM# 7 8
 [16.19] THRM# <<

PREQ#6 RN62 8P4R-2.7KR0402
 PIQ#F 1 2
 PREQ#3 3 4
 PIQ#E 5 6
 PIQ#E 7 8
 PREQ#6 <<

V_FSB_VTT
 TRMTRIP# R419 62R0402
 FERR# R420 62R0402
 TRMTRIP# <<

DMI Interface

Trace width 5 mils & 7 mils space.

GMCH breakout space 5 mils, length < 250 mils

Length matching < 5 mils

Trace Length 2" to 11"

<200mils

ICH6 integrates 20K ohm
nomial pull-up resistors

[18,19,29] LPC_AD0<
[18,19,29] LPC_AD1<
[18,19,29] LPC_AD2<
[18,19,29] LPC_AD3<
[19] LPC_DRQ0<
[18,19,29] LPC_FRAME#<

[20] AC_BHCLK<
[20] AC_RST#<
[20] AC_SDIN2<
[20] AC_SDOUT<
[20] AC_SYNC<

[26] USB4<
[26] USB4+<
[26] USB1<
[26] USB1+<
[26] USB0<
[26] USB0+<
[26] USB5<
[26] USB5+<
[26] USB2<
[26] USB2+<
[26] USB3<
[26] USB3+<
[26] USB6<
[26] USB6+<
[26] USB7<
[26] USB7+<

[26] OC#1_2<
[26] OC#3_4<

[12,18,21,24,27] SMBCLK<
[12,18,21,24,27] SMBDATA<
[12,18,21,24,27] SMB_ALERT#<
[12,18,21,24,27] SM_LINK0<
[12,18,21,24,27] SM_LINK1<
[12,18,21,24,27] LINK_ALERT#<

[24] RSMRST#<
[19] PWRBTN#<
[8,24] MS7_POK<
[28] VRM_GD<
[24,25] FP_RST#<

[14,19,24] SLP_S3#<
[24] SLP_S4#<
[24] SLP_S5#<
[29] LPCPD#<

[21] WAKE#<
[29] RI#<
[15,19] THRM#<

[8] ICH_SYNC#<
[25] SPKR<
[25] BATTLOW#<

[18] ICH_14M<
[18] USB_48<

VCC5_SB
R301 4.7KR0402
R297 10KR0402
RSMRST#<

should go high no sooner
than 10ms after both VCC3_SB
and VCC1.5_SB have reached
their nomial voltages

LPC
AC-LINK

USB

SM BUS

POWER MGMT

MISC

ICH 6
PART 2/3

P-ATA

S-ATA

GPIO

RTC

DDACK#<
DDREQ<
DIOR#<
DIOW#<
IORDY<
LDQ0_0#<
DA1<
DA2<
DCS1#<
DCS3#<

DD_0<
DD_1<
DD_2<
DD_3<
DD_4<
DD_5<
DD_6<
DD_7<
DD_8<
DD_9<
DD_10<
DD_11<
DD_12<
DD_13<
DD_14<
DD_15<

SATA_0RXN<
SATA_0RXP<
SATA_0TXN<
SATA_0TXP<
SATA_1RXN<
SATA_1RXP<
SATA_1TXN<
SATA_1TXP<
SATA_2RXN<
SATA_2RXP<
SATA_2TXN<
SATA_2TXP<
SATA_3RXN<
SATA_3RXP<
SATA_3TXN<
SATA_3TXP<

SATALED#<
GPIO26/SATA_0GP<
GPIO29/SATA_1GP<
GPIO30/SATA_2GP<
GPIO31/SATA_3GP<

BMBUSY/GPI6<
GPI7<
GPI8<
GPI9<
GPI10<
GPI11<
GPI12<
GPI13<
GPI14<
GPI15<
GPI16<
GPI17<
GPI18<
GPI19<
GPI20<
GPI21<
GPI22<
GPI23<
GPI24<
GPI25<
GPI26<
GPI27<
GPI28<
GPI29<
GPI30<
GPI31<
GPI32<
GPI33<
GPI34<

STP_PCH#<
STP_CPU#<
GPO19<
GPO20<
GPO21<
GPO22<
GPO23<
GPO24<
GPO25<
GPO26<
GPO27<
GPO28<
GPO29<
GPO30<
GPO31<
GPO32<
GPO33<
GPO34<

VCCRTC<
INTVRMEN<
RTCRST#<
RTCX1<
RTCX2<

RTCX1<
RTCX2<

RTCX1<
RTCX2<

RTCX1<
RTCX2<

RTCX1<
RTCX2<

RTCX1<
RTCX2<

RTCX1<
RTCX2<

integrated series resistors

SATA_RX#0<
SATA_RX0<
SATA_TX#0<
SATA_TX0<

SATA_RX#1<
SATA_RX1<
SATA_TX#1<
SATA_TX1<

SATA_RX#2<
SATA_RX2<
SATA_TX#2<
SATA_TX2<

SATA_RX#3<
SATA_RX3<
SATA_TX#3<
SATA_TX3<

CK_ICHSATA#<
CK_ICHSATA#<

SATALED#<
GPIO26/SATA_0GP<
GPIO29/SATA_1GP<
GPIO30/SATA_2GP<
GPIO31/SATA_3GP<

BMBUSY/GPI6<
GPI7<
GPI8<
GPI9<
GPI10<
GPI11<
GPI12<
GPI13<
GPI14<
GPI15<
GPI16<
GPI17<
GPI18<
GPI19<
GPI20<
GPI21<
GPI22<
GPI23<
GPI24<
GPI25<
GPI26<
GPI27<
GPI28<
GPI29<
GPI30<
GPI31<
GPI32<
GPI33<
GPI34<

STP_PCH#<
STP_CPU#<
GPO19<
GPO20<
GPO21<
GPO22<
GPO23<
GPO24<
GPO25<
GPO26<
GPO27<
GPO28<
GPO29<
GPO30<
GPO31<
GPO32<
GPO33<
GPO34<

SM BUS Pull-High

SMBCLK<
SMBDATA<
R494 3.3KR0402 VCC3_SB
R302 3.3KR0402 VCC3
R305 3.3KR0402 VCC3
R495 3.3KR0402 VCC3_SB

C383 C100P16X0402
C382 X_C100P16X0402

VCC3
C610 C0.1U16Y0402
C611 C0.1U16Y0402

V_1P5_CORE
For SMBus cross plane

VCC3
C48 X_C100P50X0402
For FMT

LINK_ALERT#<
SMB_ALERT#<
SM_LINK0<
SIO_PME#<
GPI6<
RI#<
BATTLOW#<
LPCPD#<
WAKE#<
SM_LINK1<

PS_DETECT<
GPI6<
GPI7<
SATALED#<

MS7_POK<
R296 10KR0402
INTRUDER#<
R295 2MR0402 VBAT

check Power on sequency (SI)

should go high no sooner
than 10ms after both VCC3
and VCC1.5 have reached
their nomial voltages

RTC BLOCK

CLR_CMOS
1-2 Normal
1-2 Clear CMOS

VCC5_SB
R496 1.2KR
R497 2.7KR
V_BAT
VBAT

S-BAT54C_SOT23
D13
R317 8.2KR
C370 C1U16X0805
C22U6.3X5
C599 X_C10U16.3X50805-1

RC filter on this line
should be 18 ~ 25ms
ADV suggestion:
R317: 8.2K, C411:2.2uF

RTCRST#<
RTCX1<
RTCX2<

RTCX1<
RTCX2<

RTCX1<
RTCX2<

RTCX1<
RTCX2<

RTCX1<
RTCX2<

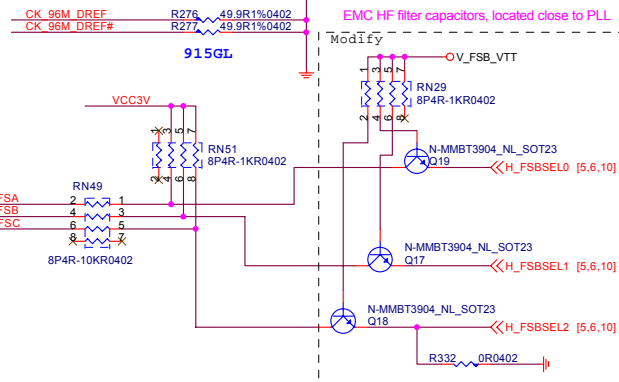
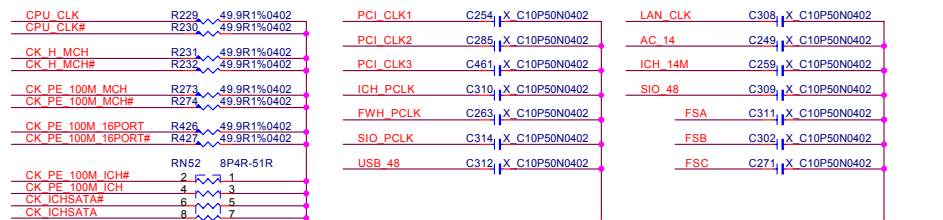
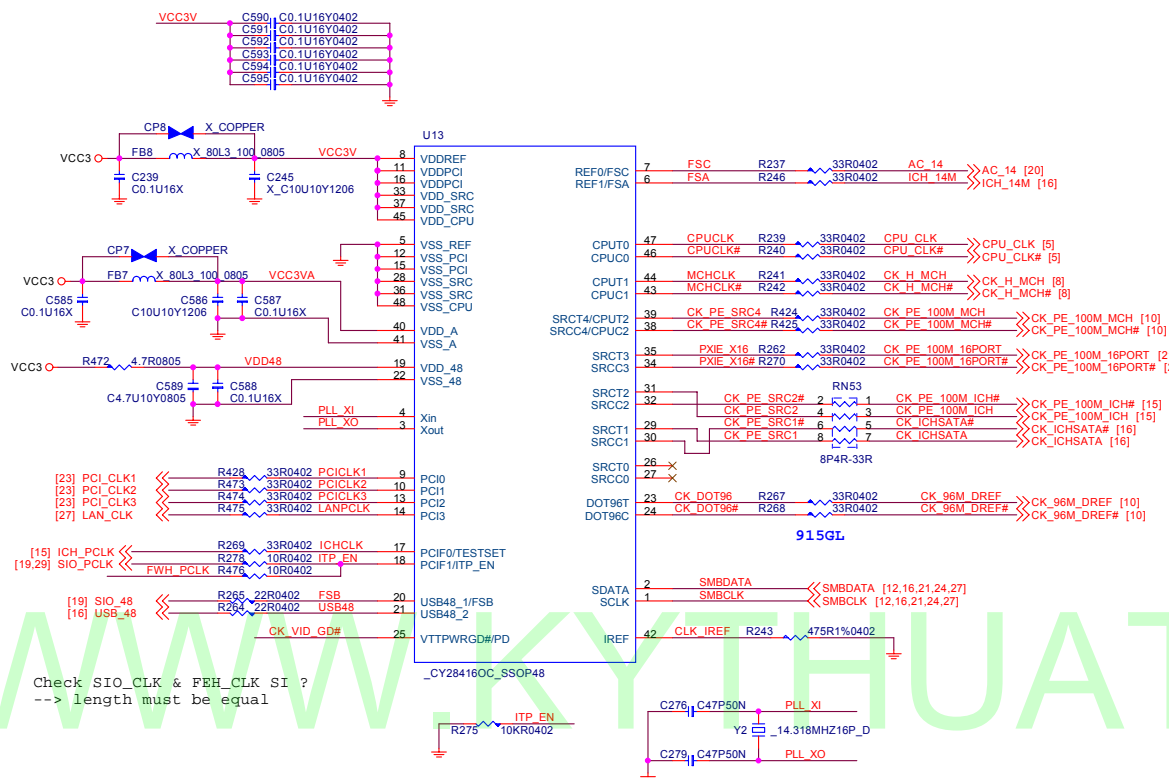
MSI MICRO-START INTL CO.,LTD.

ICH6 LPC, ATA, USB, RTC

Size Cuspm Document Number MS-7177 Rev 0A

Date: Wednesday, May 18, 2005 Sheet 16 of 33

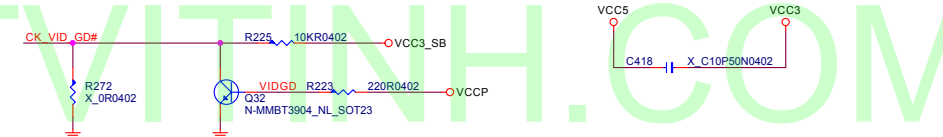
Clock Generator - CY28416



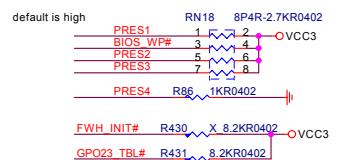
FSA	FSB	FSC	Host Clock	FSB Freq.
1	0	0	133M	533M
0	1	0	200M	800M

Other combinations are reserved.

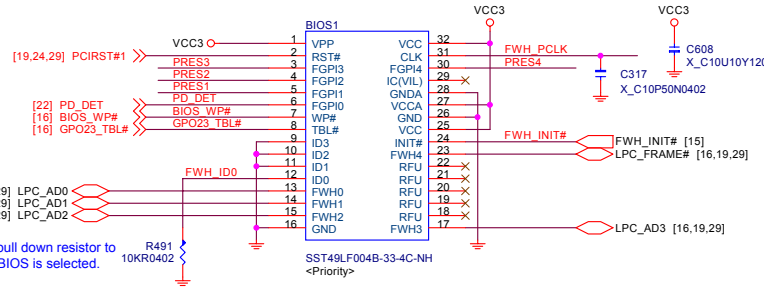
Clock Generator VTT Power Down Block



FWH Resistors

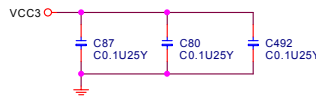


Firmware Hub (FWH)



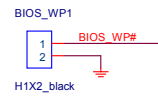
Note that use pull down resistor to identify which BIOS is selected.

FWH DECOUPLING CAPACITORS



Place Cap. as Close to FWH< 350 mil

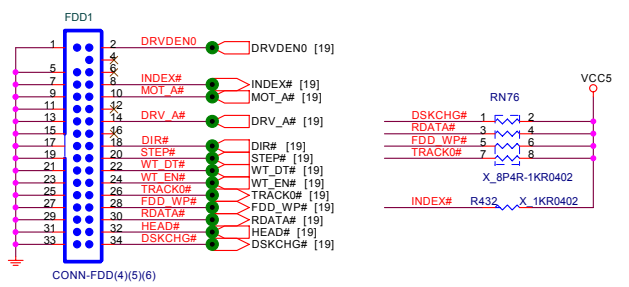
BIOS PROTECT BLOCK



BIOS_TBL#	<p>(Top Block Lock)</p> <p>When low, prevents programming to the boot block sectors at the top of the device memory.</p>
BIOS_WP#	<p>(Write Protect)</p> <p>When low, prevents programming to all but the highest addressable blocks.</p>

BIOS_TBL# always Low Only When Bootblock
needs to be flashed

FLOPPY CONNECTOR



Title			
Clock Gen. & FWH & FDD			
Size	Document Number	Rev	
Custom	MS-7177	0A	
Date:	Wednesday, May 18, 2005	Sheet	18 of 33

Schematic diagram for EMI suppression. Two signal lines, SIO_PCLK_C77 and SIO_48_C78, are shown. Each line passes through a ferrite bead (C10P50N0402) before reaching ground. The text "For EMI" is written below the diagram.



The schematic diagram illustrates the electrical connections for the Serial Port 1 and Parallel Port of the N51-09M0021-A10 module. It is divided into two main sections: SERIAL PORT 1 and PARALLAL PORT.

SERIAL PORT 1: This section shows the connection of the U1 (GD75232_SSOP20) serial-to-parallel converter. The VCC pin (1) is connected to VCC5. The GND pin (11) is connected to GND. The RIA# pin (19) is connected to RIA# (1). The CTS# pin (18) is connected to CTS# (1). The DSRA# pin (17) is connected to DSRA# (1). The SINA pin (14) is connected to SINA (1). The DCDA# pin (12) is connected to DCDA# (1). The NRTSA pin (5) is connected to NRTSA (1). The NDTRA pin (6) is connected to NDTRA (1). The NSOUTA pin (8) is connected to NSOUTA (1). The NRTSA pin (1) is connected to NRTSA (1). The NDSRA# pin (3) is connected to NDSRA# (1). The NCTSA# pin (4) is connected to NCTSA# (1). The NDSRA# pin (5) is connected to NDSRA# (1). The NCTSA# pin (6) is connected to NCTSA# (1). The NDSRA# pin (7) is connected to NDSRA# (1). The NCTSA# pin (8) is connected to NCTSA# (1). The NDSRA# pin (9) is connected to NDSRA# (1). The NCTSA# pin (10) is connected to NCTSA# (1). The NDSRA# pin (11) is connected to NDSRA# (1). The NCTSA# pin (12) is connected to NCTSA# (1). The NDSRA# pin (13) is connected to NDSRA# (1). The NCTSA# pin (14) is connected to NCTSA# (1). The NDSRA# pin (15) is connected to NDSRA# (1). The NCTSA# pin (16) is connected to NCTSA# (1). The NDSRA# pin (17) is connected to NDSRA# (1). The NCTSA# pin (18) is connected to NCTSA# (1). The NDSRA# pin (19) is connected to NDSRA# (1). The NCTSA# pin (20) is connected to NCTSA# (1).

PARALLAL PORT: This section shows the connection of the LPT1 (N51-25F0041-A10) parallel port. The SLCT pin (13) is connected to SLCT (1). The PE pin (25) is connected to PE (1). The BUSY pin (24) is connected to BUSY (1). The ACK# pin (23) is connected to ACK# (1). The PRND7 pin (22) is connected to PRND7 (1). The PRND6 pin (21) is connected to PRND6 (1). The PRND5 pin (20) is connected to PRND5 (1). The PRND4 pin (19) is connected to PRND4 (1). The PRND3 pin (18) is connected to PRND3 (1). The PRND2 pin (17) is connected to PRND2 (1). The PRND1 pin (16) is connected to PRND1 (1). The ERR# pin (15) is connected to ERR# (1). The AFD# pin (14) is connected to AFD# (1). The STB# pin (13) is connected to STB# (1).

[illegible]

LPC I/O STRAPPING RESISTOR

Diagram showing the connection of strapping resistors (R7, R19, R2, R6, R5) to VCC5 and ground, and the connection of status signals (SOUTA, SOUTB, RTSA#, DTRA#).


Chassis Intrusion

Diagram showing the connection of VBAT0 to chassis ground (CHASSIS) via resistors R3 and R4, and the connection of VBAT0 to ground via capacitors C39, C10, C49, and C8.

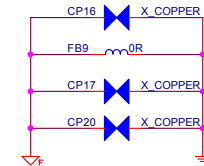
Temperature Sensor

Diagram showing the connection of the temperature sensor (TMP_VREF) to the system temperature (SYS_TMP) via resistors R48 and RT1, and the connection of the sensor to ground via capacitors C0.1U25Y and C40.

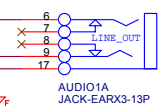
NOTE: LOCATE CLOSE STATUS PANEL

 MICRO-START INTL CO.,LTD.	
Title	
SIO, KBMS, COM, Print	
Size	Document Number
Custom	MS-7177
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Rev 0A	

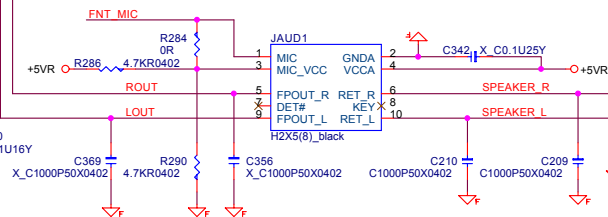
COPPER



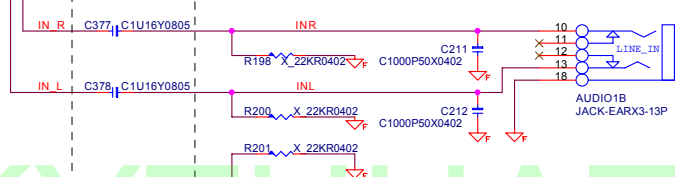
SPEAKER OUT



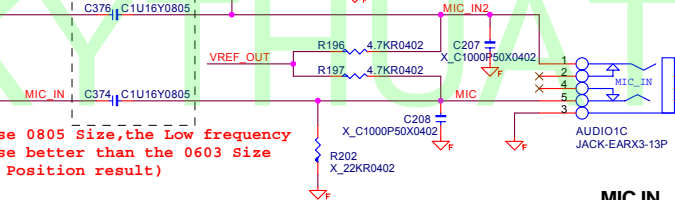
FRONT AUDIO



LINE IN

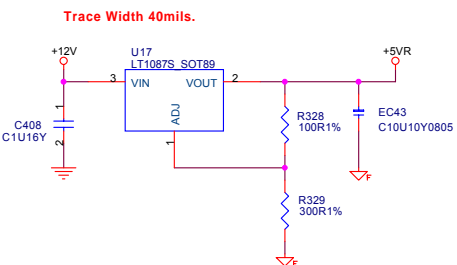


MIC IN

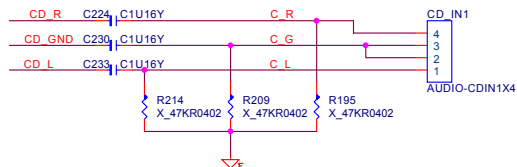


FOR LEGEND

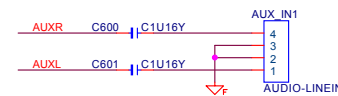
AUDIO CODE REGULATORS



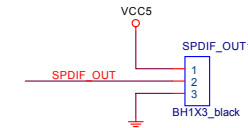
CD IN

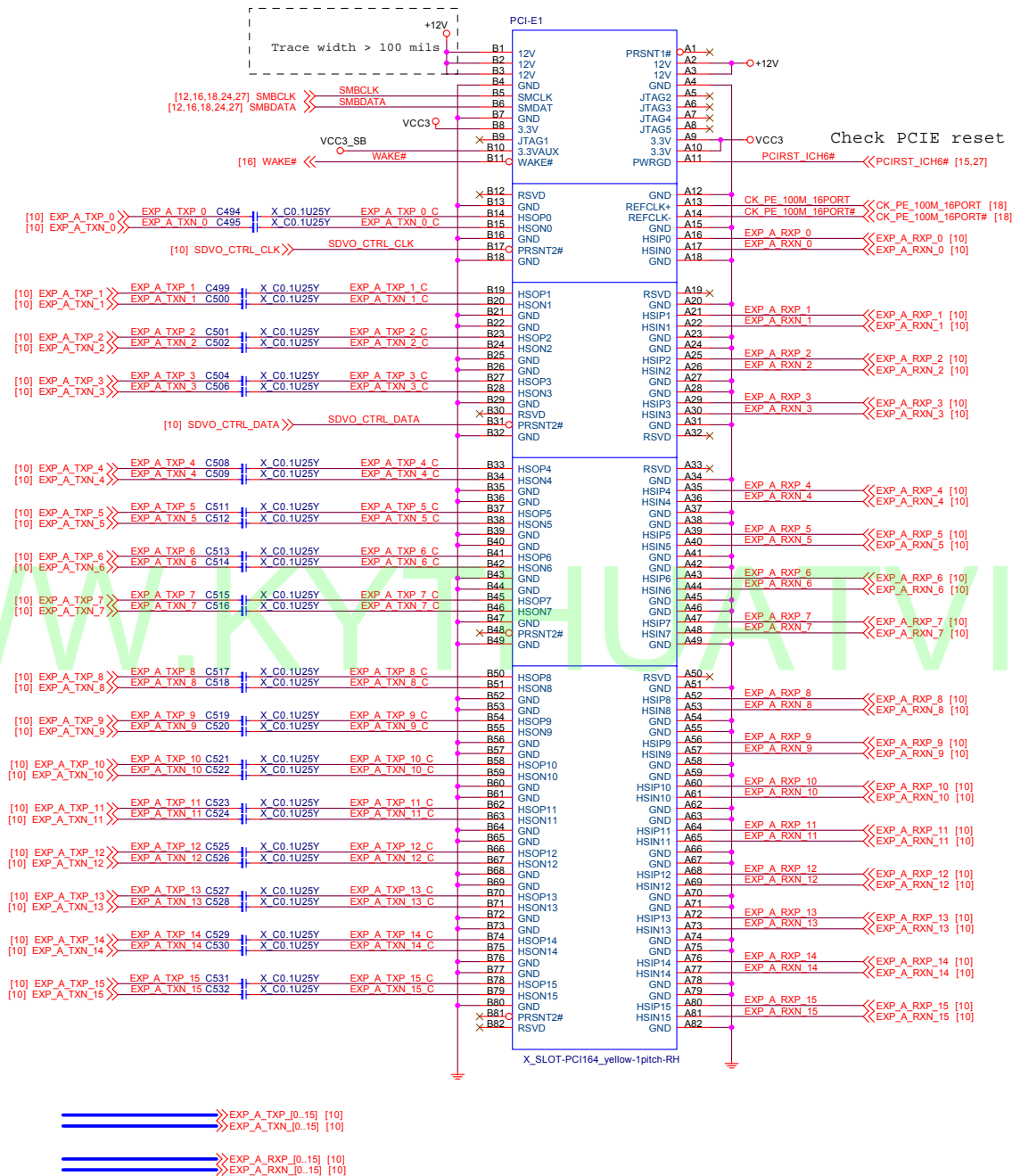


AUX IN

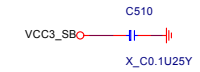
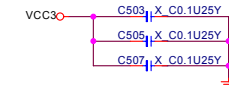
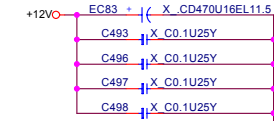


SPDIF Out





PCI EXPRESS 1-PORT



The schematic diagram illustrates the IDE1 connector pinout and its connections. The connector is labeled IDE1_0 through IDE1_40. The connections are as follows:

- IDE1_0 to IDE1_15:** These pins are connected to the IDE1_0 to IDE1_15 signals. The signals are labeled as follows:
 - IDE1_0: HD_RST#
 - IDE1_1: PD_DREQ
 - IDE1_2: PD_IOW#
 - IDE1_3: PD_IOR#
 - IDE1_4: PD_IORDY
 - IDE1_5: PD_DACK#
 - IDE1_6: IRQ14
 - IDE1_7: PD_A1
 - IDE1_8: PD_A0
 - IDE1_9: PD_CS#1
 - IDE1_10: PD_LED
 - IDE1_11: PD_DET
 - IDE1_12: PD_A2
 - IDE1_13: PD_CS#3
 - IDE1_14: PD_CS#3
 - IDE1_15: PD_CS#3
- IDE1_16 to IDE1_31:** These pins are connected to the IDE1_16 to IDE1_31 signals. The signals are labeled as follows:
 - IDE1_16: PD_DREQ
 - IDE1_17: PD_IOW#
 - IDE1_18: PD_IOR#
 - IDE1_19: PD_IORDY
 - IDE1_20: PD_DACK#
 - IDE1_21: IRQ14
 - IDE1_22: PD_A1
 - IDE1_23: PD_A0
 - IDE1_24: PD_CS#1
 - IDE1_25: PD_LED
 - IDE1_26: PD_DET
 - IDE1_27: PD_A2
 - IDE1_28: PD_CS#3
 - IDE1_29: PD_CS#3
 - IDE1_30: PD_CS#3
 - IDE1_31: PD_CS#3
- IDE1_32 to IDE1_40:** These pins are connected to the IDE1_32 to IDE1_40 signals. The signals are labeled as follows:
 - IDE1_32: PD_DREQ
 - IDE1_33: PD_IOW#
 - IDE1_34: PD_IOR#
 - IDE1_35: PD_IORDY
 - IDE1_36: PD_DACK#
 - IDE1_37: IRQ14
 - IDE1_38: PD_A1
 - IDE1_39: PD_A0
 - IDE1_40: PD_CS#1

The diagram also shows the following components and connections:

- Resistors:** R221 (4.7K), R203 (8.2K), R194 (4.7K), and R210 (10K).
- Power Supply:** VCC5 and VCC3.
- Ground:** Ground connections are shown for the IDE1_0 to IDE1_15, IDE1_16 to IDE1_31, and IDE1_32 to IDE1_40 signals.

```
IDE trace impedance: 60 ohm
width: 5 mils , spacing: 7 mils
Strobes PD_IOR# (write), PD_IORDY(read)
```

The image displays four schematic diagrams for SATA1, SATA2, SATA3, and SATA4 connections. Each diagram shows a SATA connector with pins 1-9. The connections are as follows:

- SATA1:**
 - [16] SATA_TX0 >> C358 C0.01U6X0402/20%
 - [16] SATA_TX#0 >> C357 C0.01U6X0402/20%
 - [16] SATA_RX#0 << C371 C0.01U6X0402/20%
 - [16] SATA_RX0 << C372 C0.01U6X0402/20%
- SATA2:**
 - [16] SATA_TX1 >> C350 C0.01U6X0402/20%
 - [16] SATA_TX#1 >> C349 C0.01U6X0402/20%
 - [16] SATA_RX#1 << C355 C0.01U6X0402/20%
 - [16] SATA_RX1 << C362 C0.01U6X0402/20%
- SATA3:**
 - [16] SATA_TX2 >> C327 C0.01U6X0402/20%
 - [16] SATA_TX#2 >> C328 C0.01U6X0402/20%
 - [16] SATA_RX#2 << C339 C0.01U6X0402/20%
 - [16] SATA_RX2 << C340 C0.01U6X0402/20%
- SATA4:**
 - [16] SATA_TX3 >> C320 C0.01U6X0402/20%
 - [16] SATA_TX#3 >> C321 C0.01U6X0402/20%
 - [16] SATA_RX#3 << C336 C0.01U6X0402/20%
 - [16] SATA_RX3 << C337 C0.01U6X0402/20%

Each diagram shows a ground connection at pin 9. The connectors are labeled CONN-SATA1P_orange, CONN-SATA2P_orange, CONN-SATA3P_orange, and CONN-SATA4P_orange.

VGA Connector

VCC5

3VDDCCL

3VDDCDA

CRT_HSYNC

CRT_VSYNC

V_2P5_MCH

N-2N7002_SOT23

R103 2.2KR0402

R112 2.2KR0402

R88 2.2KR0402

R109 2.2KR0402

R120 33R0402

R121 33R0402

R87 33R0402

R102 33R0402

C88 C0.1U25Y

C98 C0.1U16Y0402

C93

C113

C112

D

FS1 F-MICROSMD110

POLY SWITCH

VGA_PWR

R85 X47KR FOR ESD

VGA1

17

5

15

10

14

9

13

8

12

7

11

6

16

_CONN-VGA

5V_DCCCL

5V_DCCL

5V_DCDA

HSYNC

VSYNC

For emi : close to MH1

U905

VO4

VO5

VP

VO6

VO3

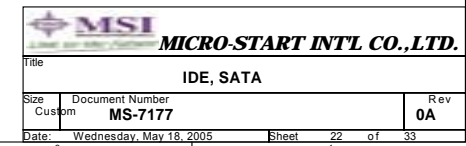
VN

VO2

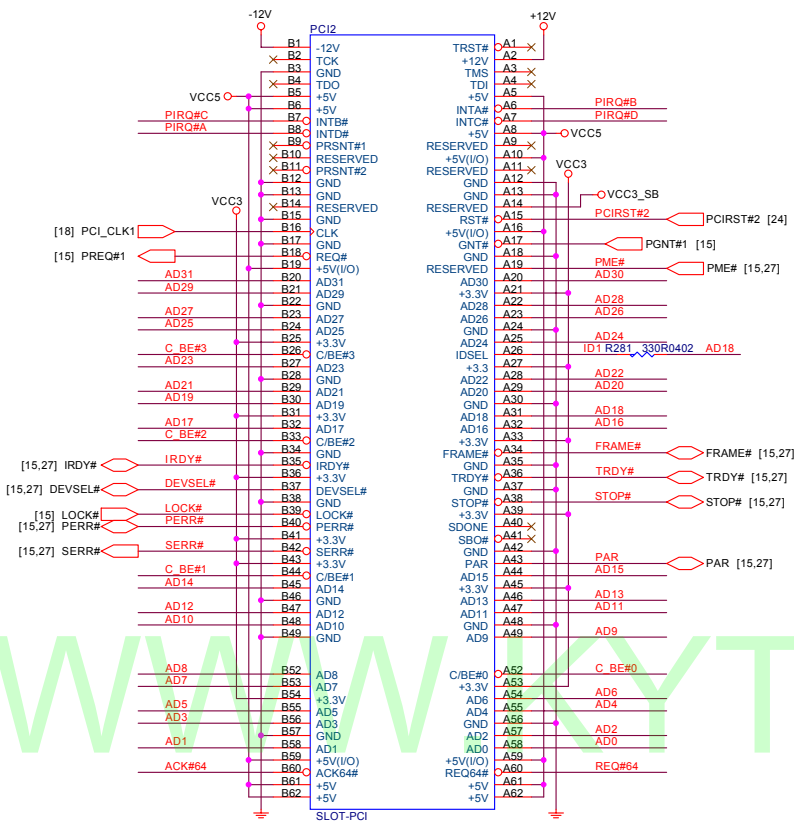
VO1

_Z_PACDND006M_MSOP8

6 Channel ESD Protection Array



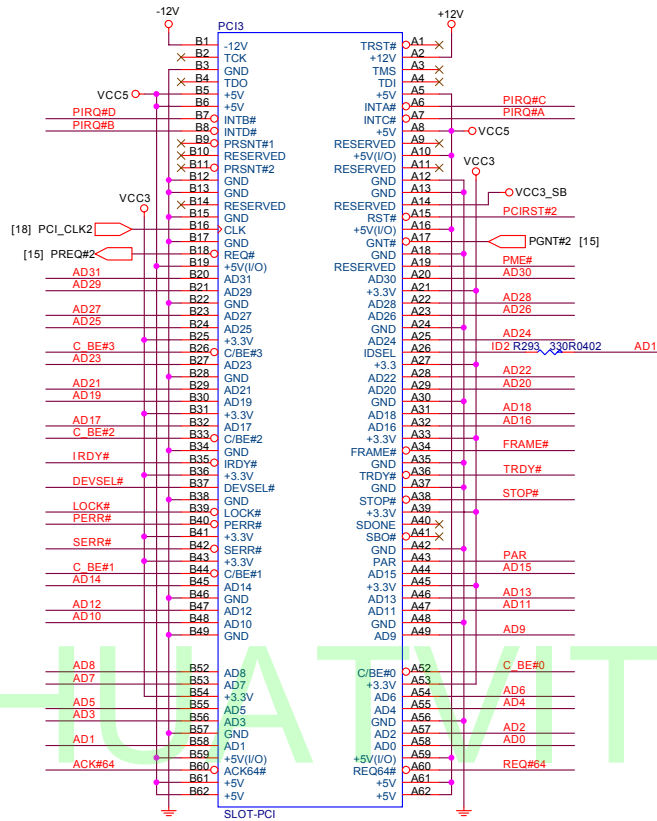
PCI SLOT 2



ISSEL = AD18
MASTER = PREQ#1
PIRQ#B

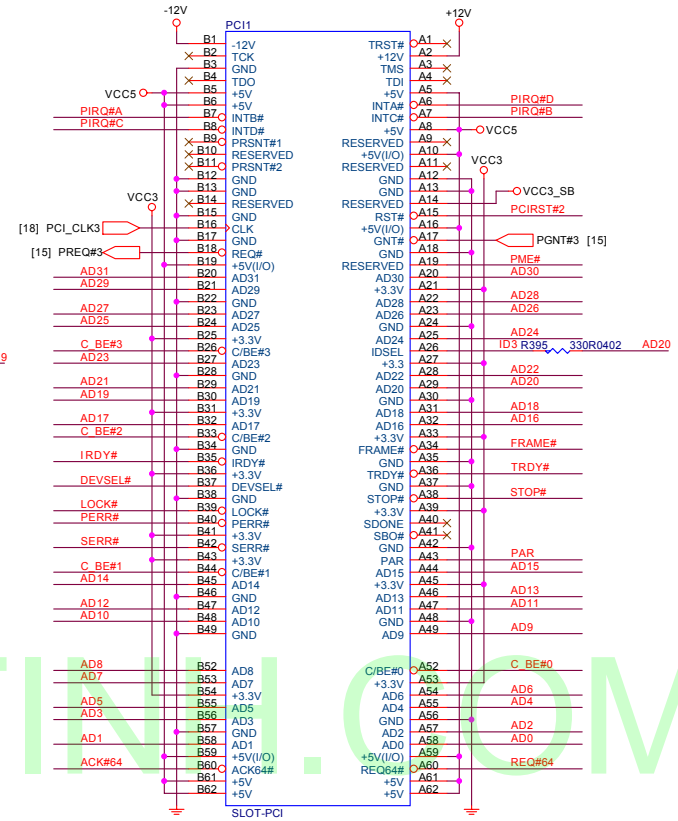
[15,27] AD[31..0] AD[31..0]
[15,27] C_BE#[3..0] C_BE#[3..0]

PCI SLOT 3



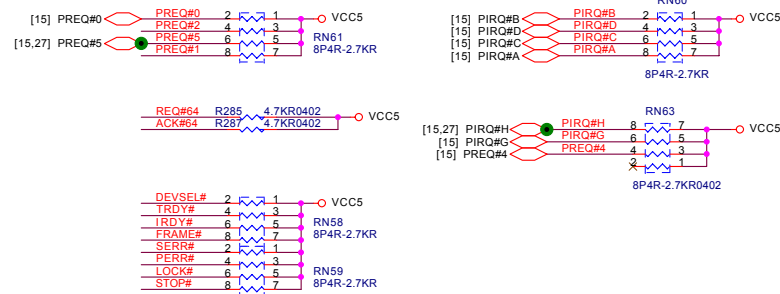
ISSEL = AD19
MASTER = PREQ#2
PIRQ#C

PCI SLOT 1



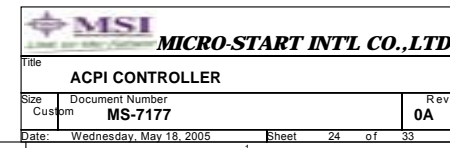
ISSEL = AD20
MASTER = PREQ#3
PIRQ#D

PCI PULL-UP / DOWN RESISTORS



VDIMM LINEAR OR PWM SELECT

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

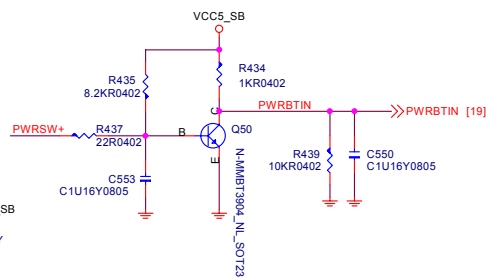


The schematic diagram illustrates the power connections for the ATX1 connector. The connector pins are numbered 1 through 12. The connections are as follows:

- Pin 1:** Connected to VCC3 (3.3V).
- Pin 2:** Connected to -12V.
- Pin 3:** Connected to GND.
- Pin 4:** Connected to P_ON (5V).
- Pin 5:** Connected to GND.
- Pin 6:** Connected to VCC5 (5V).
- Pin 7:** Connected to GND.
- Pin 8:** Connected to -5V (POK).
- Pin 9:** Connected to 5V (SVSB).
- Pin 10:** Connected to +12V.
- Pin 11:** Connected to 5V (+12V).
- Pin 12:** Connected to DET (GND).

Key components and labels include:

- Resistors:** R436 (4.7K), R440 (4.7K).
- Capacitors:** C547, C548, C549, C550, C551, C552, C553, C554, C555, C556, C561.
- Diode:** D551.
- Labels:** VCC3, -12V, GND, P_ON, VCC5, -5V, 5V, DET, +12V, PWR_OK, PS_ON#, VCC5_SB, PWR_2X12M, white, 2pitch.



The diagram illustrates the electrical connections for the H2X7(2)_yellow module. The module is represented by a yellow box labeled 'F_PANEL1' with pins 1 through 14. The connections are as follows:

- VCC5** is connected to pin 8 (HDDLED#).
- VCC5_SB** is connected to pin 12 (VCCSPK).
- FP_RST#** is connected to pin 13 (RESET).
- A 4.7K resistor (R442) is connected between **VCC5_SB** and pin 14 (GND).

A dashed green box on the right side of the diagram shows the internal structure of the module, including components like C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, and C557. The text 'For EMI' is written below the dashed green box.

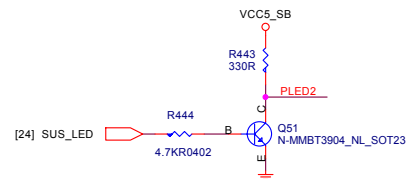
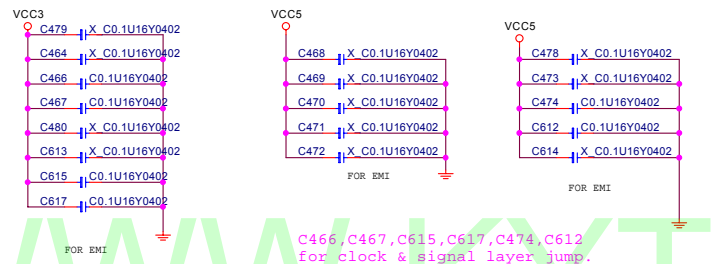
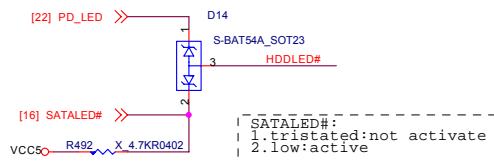
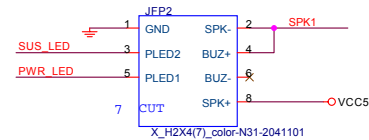


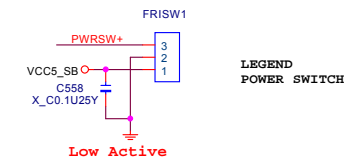
Diagram showing the connection for Pin 10 of the JFP1 connector. The pin is labeled **PWSW-** and is connected to the signal **X_H2X5(10)_black-N31-2051231**. Other pins shown include **HDDLED** (Pin 1), **HDDLED#** (Pin 3), **FP_RST#** (Pin 7), **GND** (Pin 5), **RESET** (Pin 9), **PWR** (Pins 2, 6, 8), and **SUS** (Pin 4).



R443,R445 can't remove.
Beacause LED will light when power on tranciention

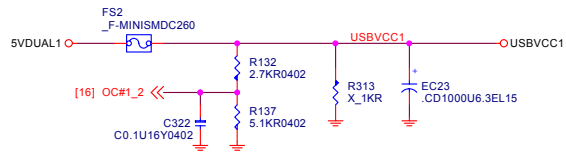
[illegible]

SPKR:ICH6 integrated pull-down,only enable at boot/reset for strapping functions; at other time is disabled.



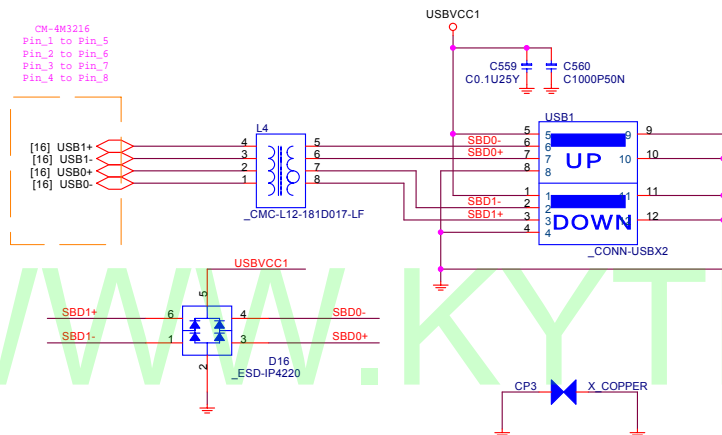
Rear USB

POWER CIRCUIT FOR USB PORT 0,1,2,3

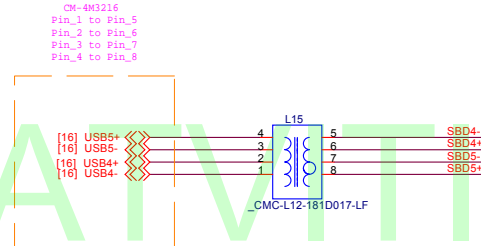


C322, C401 close to SB
EC23, EC41 close to USB connector
R313, R323: for ESD
OC# [7:0] are 3.3V level

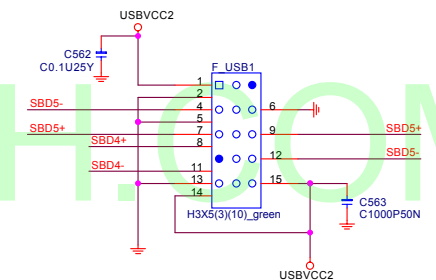
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



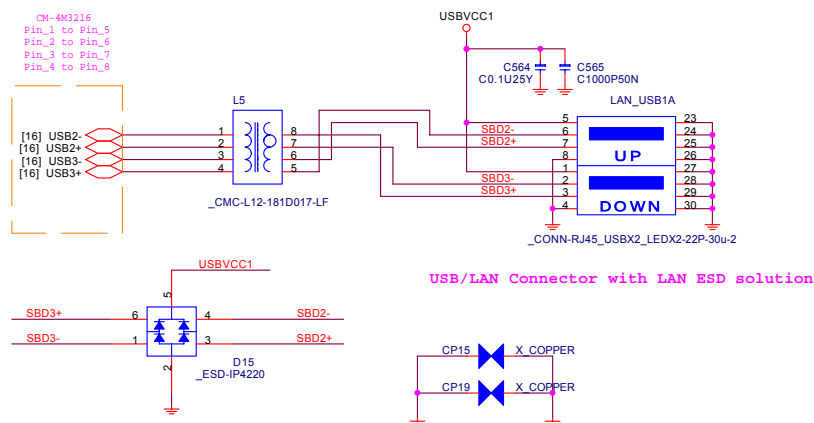
Front PANEL USB CONNECTOR FOR USB PORT 4,5



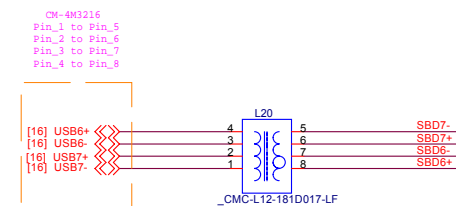
LENOVO Front USB Header



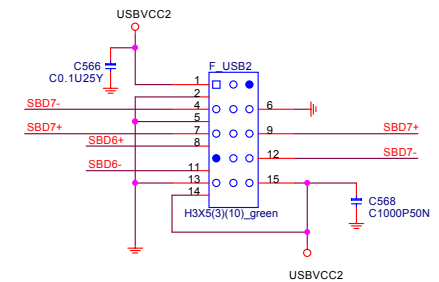
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



Front PANEL USB CONNECTOR FOR USB PORT 6,7



LENOVO Front USB Header



PCI LAN RTL8110S/8100C

R858[RSET]: 2.49K for 8110S
5.6K for 8100C

LAN EEPROM

R288 stuff 10K for 93C56

R568 X_OR

U912

AT93C46-10SI-2.7-A

R570 3.6KR1%

VDD33

DVDD

AD2

AD3

AD4

AD5

AD6

AD7

AD8

AD9

AD10

AD11

AD12

AD13

AD14

AD15

C_BE#0

C_BE#1

C_BE#2

C_BE#3

C_BE#4

C_BE#5

C_BE#6

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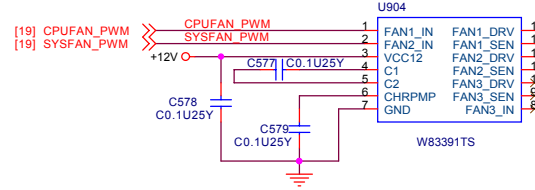
C_BE#261

C_BE#262

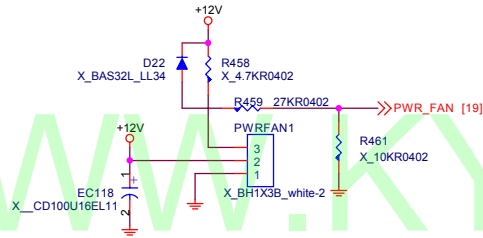
C_BE#263

C_BE#264

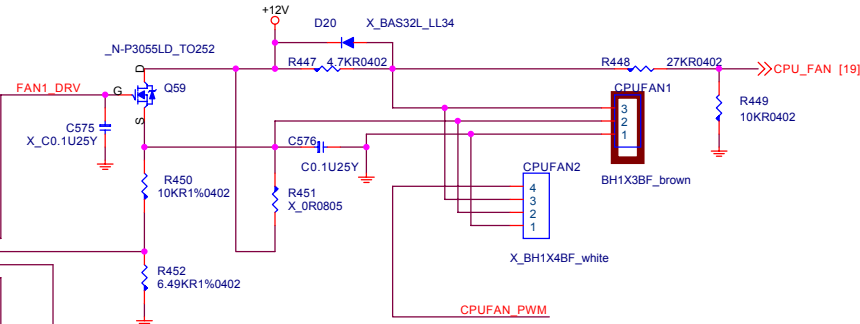
FAN CONTROL



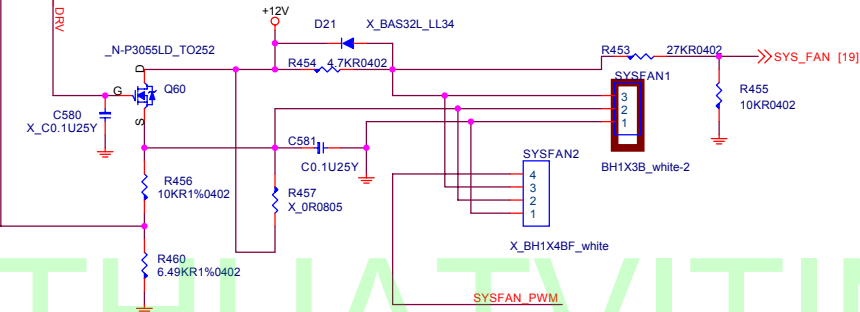
POWER FAN



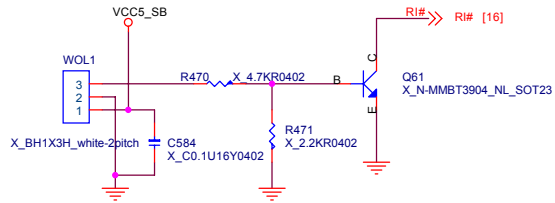
CPU FAN



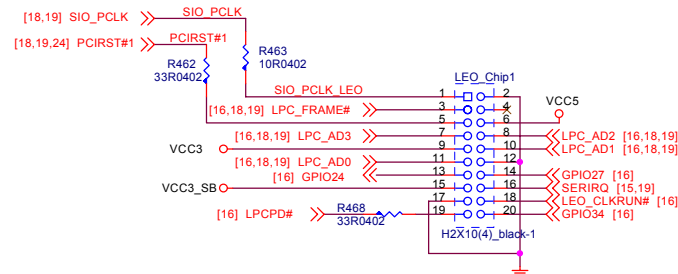
SYSTEM FAN



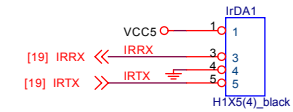
Wake on LAN



LEO HEADER

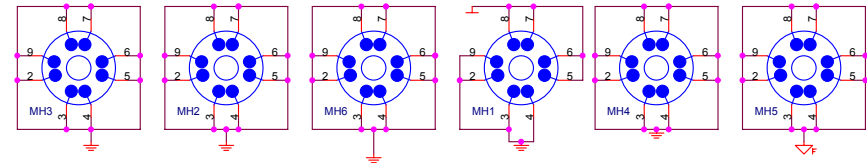
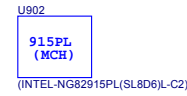
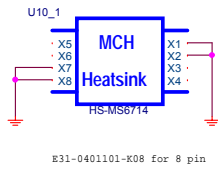


IR HEADER

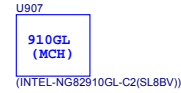
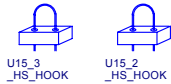
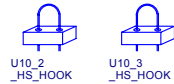


fix IR issue

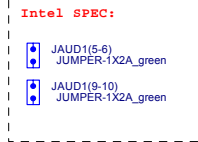
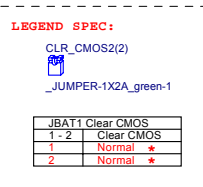
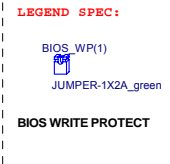
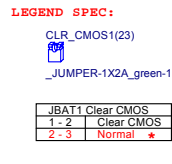
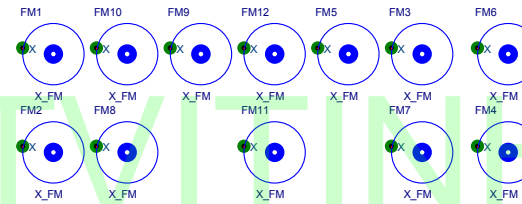
Jumper Setting / Manual Part



Mounting Holes

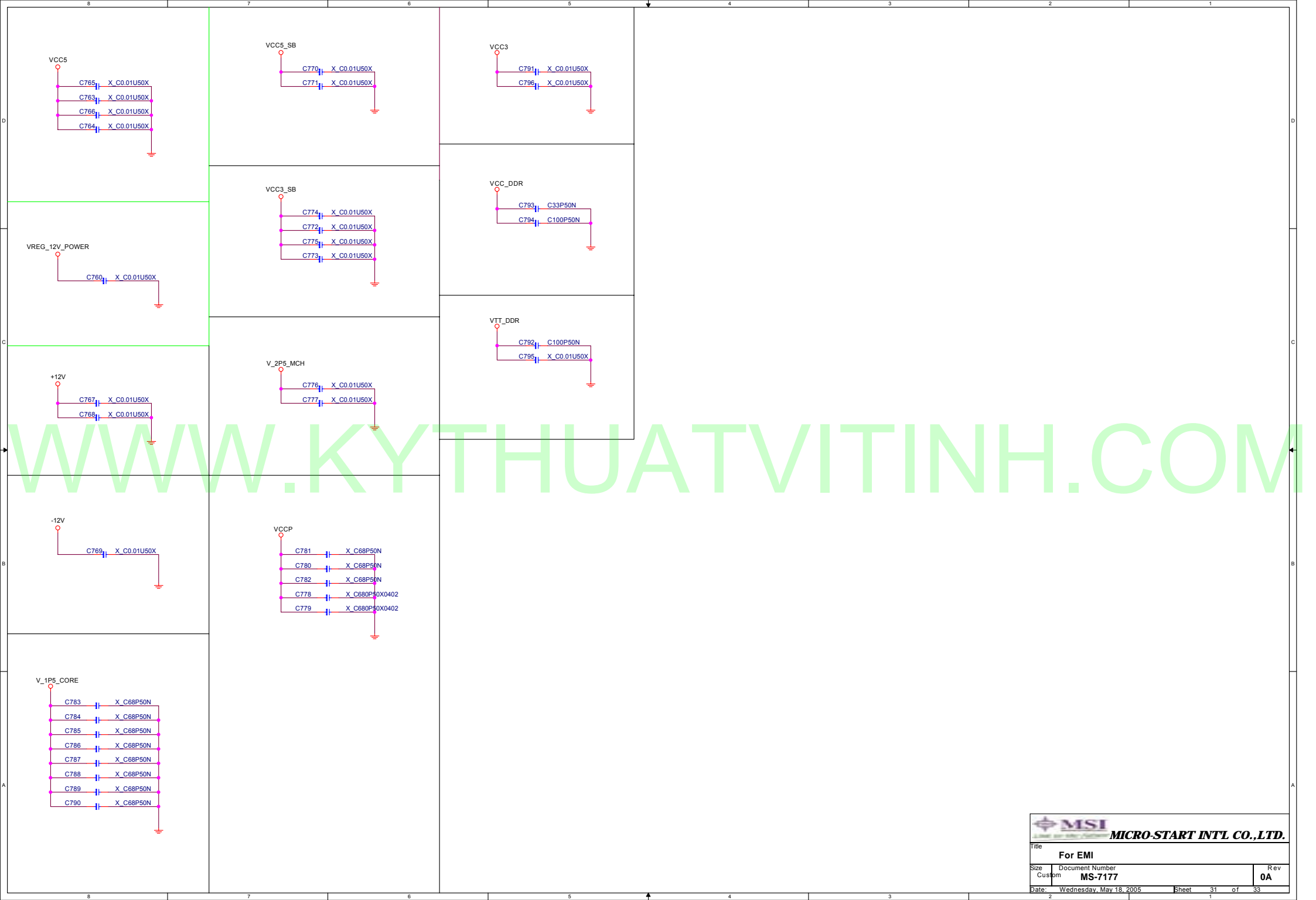


Optics Orientation Holes



Simulation





MS-7177 Config setting:

Opt Name	Function	ERP BOM	Date	Model Name	Mark

MS7177 change list

MS7171-11 change list

	Discription	Date	Page
1	Change R586 0ohm to 300ohm	2005/05/10	
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	Discription	Date	Page
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